WHAT IS CLAIMED IS:

1. A memory card comprising an erasable and programmable nonvolatile memory and a control circuit,

wherein a memory array of said nonvolatile memory includes an erasing table for storing a first flag indicating whether the memory area is a vacant area or not in every erasing unit,

wherein said memory array includes a plurality of memory cells that have a predetermined threshold voltage, and

wherein said control circuit has pre-erasing control to previously erase a predetermined memory area corresponding to the first flag indicating the vacant area irrespective of an operation instruction from the outside for instructing the address for changing the threshold voltage.

2. The memory card according to claim 1,

wherein a second flag indicating whether the memory area is in the erase condition or not corresponding to said first flag, indicating whether the memory area is a vacant area or not, is also included, and

wherein said control circuit regards, in the pre-erasing control, the memory area indicated to be a vacant area by said first flag and indicated to be a not yet erased area by said second flag, as an object area to

be erased.

3. The memory card according to claim 2, wherein said erasing table comprises an area having said first flag and said second flag.

4. The memory card according to claim 3, wherein said control circuit alters, in the pre-erasing condition, the corresponding second flag to the condition indicating the erased area after completion of the erasing process to the memory area as an erasing process object.

5. The memory card according to claim 4, wherein said control circuit performs the control to assign, to a new memory area for writing a new data to be updated, the memory area designated as a vacant area with said first flag and as an erased area with said second flag.

6. The memory card according to claim 5, wherein said control circuit updates the corresponding first flag of memory area to which an old data is written to the condition to indicate a vacant area after the data is written into said new memory area.

7. The memory card according to claim 6,

wherein said memory array of nonvolatile memory further comprises an address translation table indicating the correspondence between logical address and physical address of memory area, and

wherein said control circuit updates, after the data

is written to said new memory area assigned on the basis of said first and second flags, said address translation table through correspondence between the physical address of memory area to which the data is written and the logical address before the update of the corresponding first flag to the condition to indicate a vacant area.

8. The memory card according to claim 1, wherein said control circuit executes said pre-erasing control in response to the power-on of the memory card.

9. The memory card according to claim 1, further comprising a cipher arithmetic processing circuit, wherein said control circuit executes said pre-erasing control in parallel to the cipher arithmetic process executed with said cipher arithmetic processing circuit in response to a predetermined security command.

10. The memory card according to claim 1, wherein said control circuit executes said pre-erasing control in response to a predetermined exclusive command.

11. The memory card according to claim 1, wherein said control circuit starts said pre-erasing control in response to the completion of command process.

12. The memory card according to claim 11, wherein when an instruction by another command is issued before or after the start of the erasing operation by said pre-erasing control, the process of the relevant command is executed

preferentially.

13. A memory card comprising an erasable and programmable nonvolatile memory and a control circuit,

wherein a memory array of said nonvolatile memory is provided with a flag information area to store the flag information indicating whether a memory area is erasable or not in every erasing unit and is also provided with a plurality of memory cells having a threshold voltage within one of a plurality of threshold voltage ranges, and

wherein said control circuit executes the erasing control for erasing the erasable memory area designated with said flag information in response to the command which is different from the command indicating the address for updating the threshold voltage of memory cell.

14. A memory card comprising an erasable and programmable nonvolatile memory and a control circuit,

wherein a memory array of said nonvolatile memory includes a flag information storage area for storing the flag information indicating whether a memory area is erasable or not in every erasing unit, and

wherein said control circuit executes an erasing control for erasing the erasable memory area designated with said flag information during the period in which said control circuit does not execute an operation corresponding to the command supplied from the outside.

15. The memory card according to claim 14, wherein said flag information comprises a pair of the first flag indicating whether the memory area is a vacant area or not in every erasing unit and the second flag indicating whether the memory area is erased or not corresponding to the first flag indicating whether the memory area is a vacant area or not.

16. The memory card according to claim 15, wherein said control circuit designates, as an object area of erasing process, the memory area which is designated, in said erasing control, as an vacant area with said first flag and as a non-erased area with said second flag.

17. The memory card according to claim 16, wherein said control circuit alters, in said erasing control, the corresponding second flag to the condition indicating an erased area after completion of the erasing process to the memory area as an object area of said erasing process.

18. The memory card according to claim 17, wherein said control circuit executes a control for assigning the memory area designated as a vacant area with said first flag and as an erased area with said second flag to a new memory area for writing data to be updated.

19. The memory card according to claim 18, wherein said control circuit updates the corresponding first flag of memory area to which an old data is written to the condition

indicating a vacant area after the data is written to said new memory area.

20. The memory card according to claim 19, wherein the memory array of said nonvolatile memory further includes an address translation table indicating the correspondence between the logical address and physical address of the memory area, and

wherein said control circuit updates, after the data is written to said new memory area assigned on the basis of said first flag and said second flag, said address translation table through correspondence between the physical address of memory area to which the data is written and the logical address before the corresponding first flag is updated to the condition indicating a vacant area.